

Fig. 1
(Prior Art)

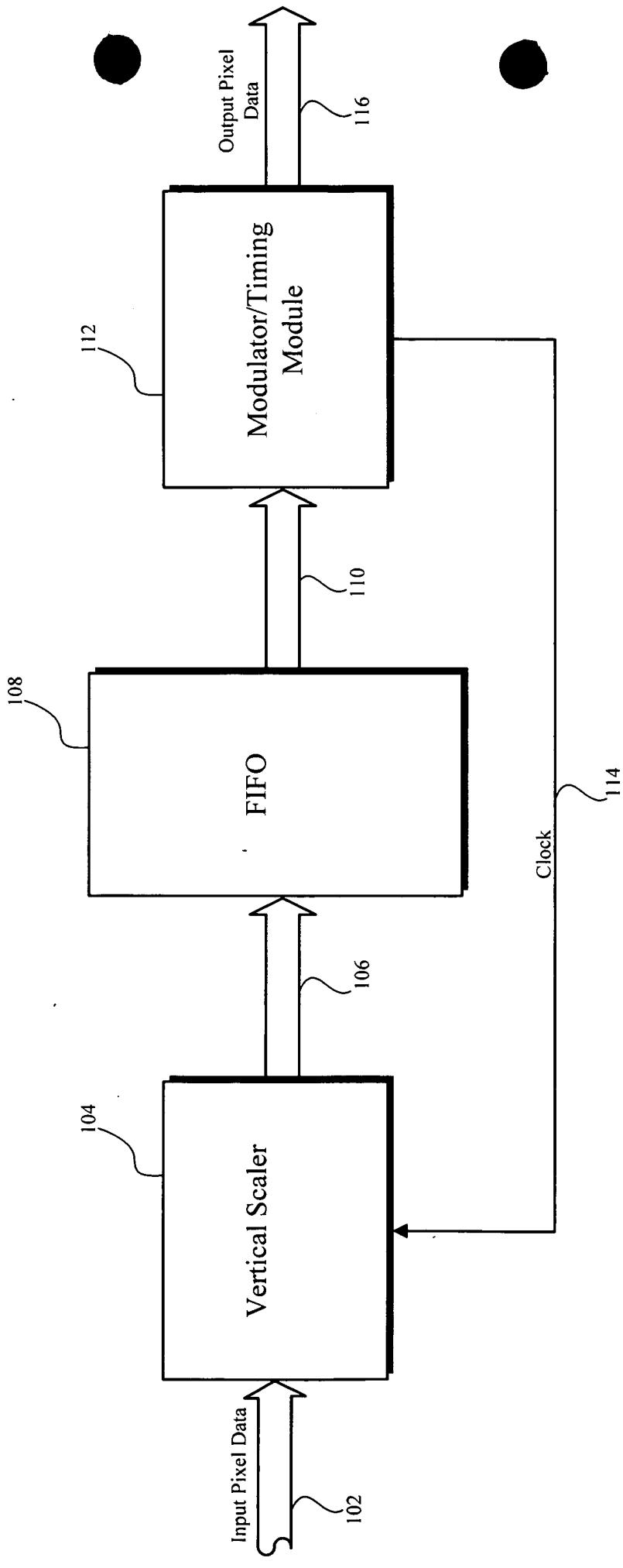


Fig. 2

Input Pixel Data
HSYNC Signal
VSYNC Signal
Blanking Signal

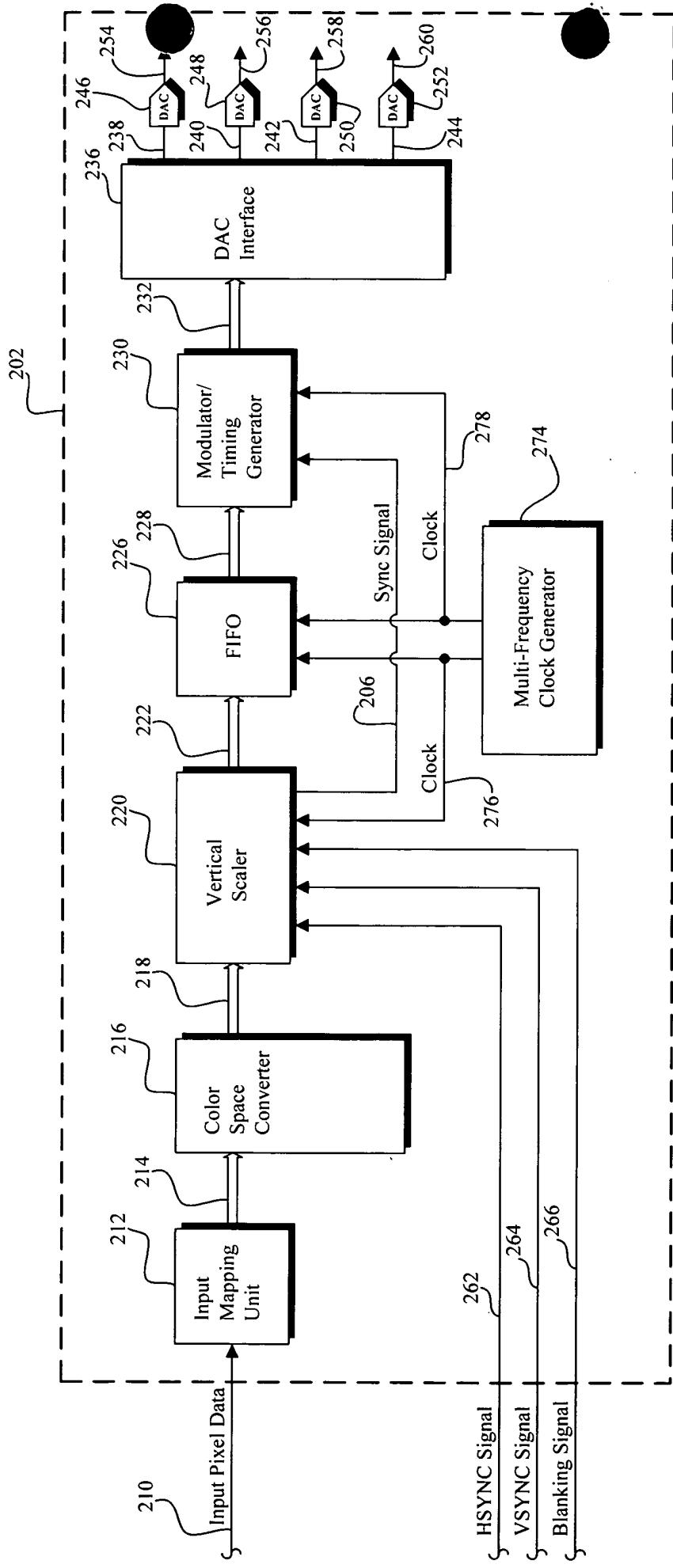


Fig. 3A

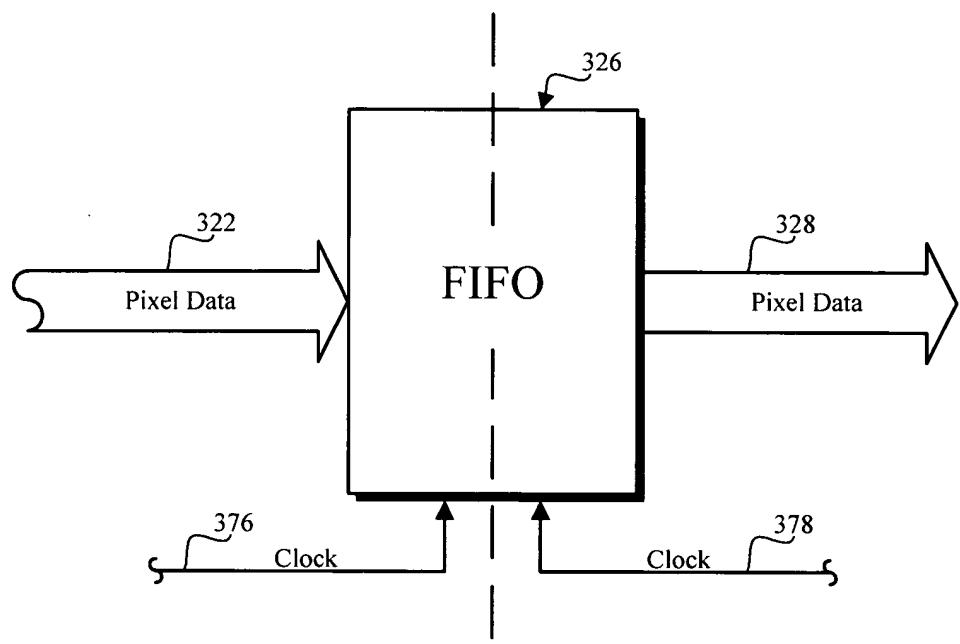


Fig. 3B

